Exhibit E

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

AFFIDAVIT

Commissioner of Patents and Trademarks
Washington, D.C. 20231

Commissioner:

I, John Giorgis, Jr., herewith affirm as follows.

(A) I was born on May 15, 1925; and I am a U.S. Citizen.

(B) I presently live at 1047 Piermont Road, South Euclid, Ohio 44121.

(C) In 1950 I received a B.E.E. Degree in Electrical Engineering from Catholic University of America, Washington, D.C.;

In 1956 I received an MSE Degree in Electrical Engineering from Union College and University, Schenectady, N.Y.; and

In 1962 I received my Professional Engineering License from the State of New York.

(D) I have practiced Electrical and Electronics Engineering since 1950, as follows.

1. Between September 1950 and September 1951 I was on the General Electric Company (G.E.) engineering training program with assignments in magnetic amplifiers, jet engine instrumentation, and power transformers.

2. Between September 1951 and October 1959 I was with G.E.'s Aeronautical and Ordnance Systems Division where I was responsible for the hardware design of the magnetic amplifier reactor control system of the atomic submarine Sea Wolf. I also did transistor control and circuit design for military systems.

3. Between October 1959 and February 1968 I was an Applications Engineer with G.E.'s Semiconductor Products Department, specializing in semiconductor applications for the military and industrial markets.

In addition, I designed a number of thick film and monolithic integrated circuits for these markets. I was co-author of the sixth and seventh editions of the G.E. Transistor Manual and of the Tunnel Diode Manual.

4. Between February 1968 and October 1976 I was a Consulting Engineer at G.E.'s Heavy Military Electronic Systems Department, where I was responsible for the Independent Research and Development Microelectronics Programs. These programs included thick film material and process studies, the design and application of custom thick film and monolithic integrated circuits.

5. Between October 1976 and April 1988 (when I retired) I was a Consulting Engineer and Technical Manager at G.E.'s Lighting Business Group in Cleveland, Ohio, designing and evaluating electronic high frequency ballasts for fluorescent and metal halide lamps.

I am the holder of three patents on inverter configurations for fluorescent lamps.

In addition, I performed research and development on the high frequency starting and running requirements of fluorescent lamps.

(E) In total, I have spent more than 10 years in the design, development, construction, testing and evaluation of electronic power supplies in general and electronic inverter-type power supplies in particular, and I have accumulated substantial experience in the art of power supplies, particularly electronic inverter-type power supplies and electronic inverter-type ballasts for fluorescent lamps.

Consequently, I believe I have at least ordinary skill in the art of electronic inverter-type power supplies, particularly as used in connection with lighting products and systems.

(F) I have read, and I am familiar with the teachings of, each one of the prior art references identified on page 3 hereof.

Prior Art References

* U.S. Patent No. 1,292,659 to Speed;
* U.S. Patent No. 2,587,169 to Kivari;
* U.S. Patent No. 2,721,929 to Schwartz et al.;
* U.S. Patent No. 2,923,856 to Greene et al.;
* U.S. Patent No. 2,965,856 to Roesel;
* U.S. Patent No. 3,368,164 to Shapiro;
* U.S. Patent No. 3,496,518 to Neumann et al.;
* U.S. Patent No. 3,541,504 to Bush;
* U.S. Patent No. 3,525,012 to Dimitracopoulos et al.;
* U.S. Patent No. 3,679,931 to Powell;
* U.S. Patent No. 3,681,654 to Quinn;
* U.S. Patent No. 3,710,177 to Ward;
* U.S. Patent No. 3,727,104 to Neal et al.;
* U.S. Patent No. 3,801,865 to Roberts;
* U.S. Patent No. 3,835,333 to Balan;
* U.S. Patent No. 3,868,561 to Matthes;
* U.S. Patent No. 3,906,337 to Depenbrock;
* U.S. Patent No. 3,939,362 to Grimes et al.;
* U.S. Patent No. 3,996,493 to Davenport et al.;
* U.S. Patent No. 4,001,571 to Martin;
* U.S. Patent No. 4,008,414 to Agnew;
* U.S. Patent No. 4,057,750 to Elms et al.;
* U.S. Patent No. 4,100,476 to Ghiringhelli;
* U.S. Patent No. 4,104,715 to Lawson;
* U.S. Patent No. 4,151,445 to Davenport et al.;
* U.S. Patent No. 2,158,793 to Lewis;
* U.S. Patent No. 4,184,128 to Nilssen;
* U.S. Patent No. 4,207,497 to Capewell et al.;
* U.S. Patent No. 4,207,498 to Spira et al.;
* U.S. Patent No. 4,260,943 to Zaderej et al.;
* U.S. Patent No. 4,262,327 to Kovacik et al.;
* U.S. Patent No. 4,277,726 to Burke;
* U.S. Patent No. 4,277,728 to Stevens;
* U.S. Patent No. 4,293,799 to Roberts;
* U.S. Patent No. 4,295,079 to Otsuka et al.;
* U.S. Patent No. 4,300,073 to Skwirut et al.;
* U.S. Patent No. 4,307,353 to Nilssen;
* U.S. Patent No. 4,330,736 to Perper;
* U.S. Patent No. 4,347,460 to Latassa et al.;
* U.S. Patent No. 4,354,120 to Schornack;
* U.S. Patent No. 4,367,434 to Miller;
* U.S. Patent No. 4,386,292 to Rothwell et al.;
* U.S. Patent No. 4,406,976 to Wisbey et al.;
* U.S. Patent No. 4,414,617 to Galindo;
* U.S. Patent No. 4,438,372 to Zuchtriegel;
* U.S. Patent No. 4,443,778 to Mewissen;
* U.S. Patent No. 4,463,277 to DeCaro;
* U.S. Patent No. 4,464,606 to Kane;
* U.S. Patent No. 4,499,403 to Leppelmeier et al.;
* U.S. Patent No. 4,503,363 to Nilssen;
* U.S. Patent No. 4,504,895 to Steigerwald;
* U.S. Patent No. 4,507,698 to Nilssen;
* U.S. Patent No. 4,508,996 to Clegg et al.;
* U.S. Patent No. 4,538,095 to Nilssen;
* U.S. Patent No. 4,560,908 to Stupp et al.;
* U.S. Patent No. 4,613,943 to Pacholok;
* U.S. Patent No. 4,684,850 to Stevens;
* U.S. Patent No. 4,692,667 to Nilssen;
* U.S. Patent No. 4,731,551 to Gibbs et al;
* Canadien Patent No. 633,937 to Waller et al.
* Japanese Patent No. 57-135689 to Matsushita; (Abstract Only)
* French Patent No. 77 03324 to Peuscet;
* Pages 44-50, IEEE Spectrum, February, 1969: "Lethal electric currents" by Dalziel;
* Pages 130-133, PCI April 1983 PROCEEDINGS, by Baker;
* Pages 18-23, Lightng & Desgn Applications, March 1976;
* Page 148, Electronic Design 24, November 22, 1975;

(G) I have been informed to the effect that:

(1) the Commissioner rejected certain claims in an application for a patent for the reason that the Commissioner held the claimed invention to be obvious over prior art;

(2) as evidence of obviousness, the Commissioner cited the following prior art reference, a copy of which has been received by me:

U.S. Patent No. 4,207,498 to Spira et al.;

(3) the Commissioner held that the teachings in the cited Spira patent, when modified and/or adapted on basis of prior known art, rendered the claimed invention obvious;

(4) more particularly, the Commissioner held that by making -- on the basis of prior known art -- an obvious and desirable modification and/or application of the teachings of Spira, the claimed invention would result;

(5) in other words, the Commissioner held that, in view of prior known art, the claimed invention merely constitutes an obvious modification and/or application of Spira's teachings.

(H) I have not seen the application for patent identified in section (G) above, nor have I seen the claims thereof. More particularly, I have not received a description of the claimed invention.

(I) I have been requested:

(1) to carefully study and consider the cited reference in light of the situation described in section (G) above;

(2) to identify each and every instance of what -- in view of art known to me prior to February 1, 1990 -- I see as a desirable obvious modification and/or application of Spira's teachings;

(3) to express in writing each one of those obvious desirable modifications and/or applications.

(J) I have performed the study and consideration requested of me in section (I) above, having spent therefor an amount of time that I judged to be reasonable; and I herewith set forth in writing each and every one of those desirable obvious modifications and/or applications, as follows:

(1) Instead of the inverter circuit shown in figure 3, use a half-bridge or full-bridge circuit where the energy for the negative half-cycle is respectively derived from the bridge capacitors or directly from the d.c. bus, 50 and 51, instead of from the output network components 54 and 55.

(2) The turn-on and turn-off times of the inverter SCR's comprise 14-18% of the cycle time. Consequently the output voltage will change due to temperature and unit to unit variations. Instead, use high power fast switching bipolar power transistors or power FET's.

(3) Transformer 75 in figure 4 is a voltage transformer since the primary winding is connected across lamp 70. Instead, make transformer 75 a current transformer with three isolated windings for supplying electrode heating current.

(4) Because of the high currents in windings 56 and 58 of transformer 57 in Figure 3, transformer 57 must be designed to minimize the leakage inductance between windings 56 and 58 in order to minimize the variation of output voltage as a function of load (the number of ballasts and lamps). This can be mitigated by using multiple output windings if it is a problem.

(5) To maximize the system efficiency, the inductors 55 and 76 and transformer 57 should be wound with Litz or multiple strand wire in order to minimize the a.c. resistance losses due to the proximity effect. (This effect reduces the conductor cross-section due to the current magnetic field and is not the well known skin effect.)

(6) Capacitors 54, 72 and 73 should be made of low loss dielectric material such as polypropelene or mica.

(7) Experiments have shown that the line power factor correction circuit in Figure 5 is sensitive to the amount of power being drawn from the d.c. bus 50 and 51. While an adequate power factor can be obtained at a given load, as ballasts and

lamps are removed or added or if the lamps are dimmed, the line power factor will decrease. Other line power factor correction approaches would be the high frequency valley fill technique or an active power factor correction circuit. The line power factor correction of these circuits is much less sensitive to changes in the load than the circuit shown in the figures.

(8) If the wire to wire or wire to conduit capacitances are still too high using the thick insulation shown in Figure 2, use thin insulation on the conductors and insulated discs appropriately spaced to separate the conductors from each other and the conduit. The capacitance will be reduced because the dielectric constant of air is one and that of most insulation materials is approximately three or above.

John Giorgis, Jr.

STATE OF OHIO)
) ss
COUNTY OF Cuyahoga)

Sworn to and subscribed before me this 12th day of February, 1990.

Notary Public